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	Subsystem/Office Tracker Subsystem	
Document Title **LAT Tracker Readout Controller Chip Wafer Test Procedure**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Tracker Readout Controller Chip Wafer Test Procedure

CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
v1.0	October 14, 2001	First version
v2.0	October 30, 2001	Detailed test procedure added
v3.0	November 9, 2001	Reformatted; more tests added
v4.0	June 20, 2002	Test procedure polished

Contents

1 Purpose

This report serves to document the test plan of the GLAST LAT Tracker Readout Controller (GTRC) ASIC wafers. These tests are carried out on all ASIC's on all wafers for initial prototype assemblies and for TMCM assemblies for GLAST LAT Tracker production.

2 Scope

The GLAST LAT Tracker will be instrumented with about 80 m^2 of silicon strip detectors (SSD) and nearly 900,000 channels of electronics. The SSD's are assembled onto the two sides of composite "tray" panels, of which 19 are stacked into each of the 18 towers. Each layer of SSD's is read out by an electronics module (TMCM), mounted on the edge of the tray panel. Extensive testing of the electronics is done during assembly at the component level (ASIC and TMCM) and at the tray level. The hardware systems for those tests are described in [11]. The procedures for wafer testing of the ASIC's to be mounted on TMCM's are documented in this document and [15]. The procedures for the electrical testing of the TMCM's after all components have been mounted and wire bonding within the TMCM is complete is documented in [16]. This plan covers the electrical testing of the tracker readout controller ASIC wafers before the wafers are diced into chips. The environmental and electrical test plans of the completed towers are specified in [13] and [17].

3 Definitions

3.1 Acronyms

ASIC — Application Specific Integrated Circuit
GLAST — Gamma-ray Large Area Space Telescope
GTFE — GLAST Tracker Front-end Electronics
GTRC — GLATT Tracker Readout Controller
LAT — Large Area Telescope
PWB — Printed Wiring Board
SSD — Silicon Strip Detector
TEM — Tower Electronics Module
TMCM — Tracker Multi-Chip Module

3.2 Names of Signal lines

Signal name	Meaning
TREQ_IN	LVDS pair of TREQ_INP and TREQ_INM
RD_IN	LVDS pair of RD_INP and RD_INM
NTOKEN	LVDS pair of NTOKENP and NTOKENM
NTOKEN_OUT	LVDS pair of NTOKEN_OUTP and NTOKEN_OUTM
NSDATA_IN	LVDS pair of NSDATA_INP and NSDATA_INM
NSDATA	LVDS pair of NSDATAP and NSDATAM
NSCMD	LVDS pair of NSCMDP and NSCMDM
CLK	LVDS pair of CLKP and CLKM
NTACK	LVDS pair of NTACKP and NTACKM
NTREQ	LVDS pair of NTREQP and NTREQM
NRESET	LVDS pair of NRESETP and NRESETM
CLKB	LVDS pair of CLKBP and CLKBM
SCMD_OUT	LVDS pair of SCMD_OUTP and SCMD_OUTM
TACKB	LVDS pair of TACKBP and TACKBM

3.3 Names of GTRC Commands

Command name	Function code	Meaning of the command
NOP	00000	No operation
RST_GTRC	00001	Reset GTRC chip
READ_EVENT	00100	Start the event read-out sequence
LD_GTRC_REG	01000	Load the GTRC Configuration Register
LD_GTFE_SYNC	01001	Load the GTFE Sync Register
RD_GTRC_REG	10000	Read the GTRC Configuration Register
RD_GTFE_SYNC	10001	Read the GTFE Sync Register

3.4 Names of GTFE Commands

Command name	Function code	Meaning of the command
FE_NOP	00000	No operation
FE_RST_CHIP	00010	Reset chip
FE_CALIBRATE	00011	Generate a calibration strobe
FE_READ_EVENT	00100	Start the event read-out sequence
FE_LD_CHN_MSK	01000	Load GTFE Channel Mask
FE_LD_CAL_MSK	01001	Load GTFE Calibration Mask
FE_LD_TRG_MSK	01010	Load GTFE Trigger Mask
FE_LD_TH/C_DAC	01011	Load GTFE Threshold and Calibration DAC's
FE_LD_MUTE	01100	Load GTFE MODE register
FE_RD_CHN_MSK	10000	Read GTFE Channel Mask
FE_RD_CAL_MSK	10001	Read GTFE Calibration Mask
FE_RD_TRG_MSK	10010	Read GTFE Trigger Mask
FE_RD_TH/C_DAC	10011	Read GTFE Threshold and Calibration DAC's
FE_RD_MUTE	10100	Read GTFE MODE register

3.5 Names of GTRC configuration register bits

Name	Bit	Function
LD_FT	33	Enables loading FORCE_NO_ERR and TOT_EN bits
LD_DELAY	32	Enables loading READ_DELAY bit
LD_STRETCH	31	Enables loading OR_STRETCH bits
LD_CNT	30	Enables loading GTFE_CNT bits
LD_SIZE	29	Enables loading SIZE bits
SUM_ERR	28	Stores logical OR of TAG_ERR, TOK_ERR, TRIG_ERR, DAT_ERR, and CMD_ERR (read only)
CMD_ERR	27	Stores a command parity error (read only)
DAT_ERR	26	Stores a data parity error (read only)
TRIG_ERR	25	Stores a trigger parity error (read only)
TOK_ERR	24	Stores a token parity error (read only)
TAG_ERR	23	Stores a tag error (read only)
SHIFT_MODE	22	Stores a logical state of the bonding pad to determine side (read only)
TOT_EN	21	Enables TOT delay
FORCE_NO_ERR	20	Forces normal event read-out
READ_DELAY	17–19	Defines delay of FE_READ_EVENT command in reference to READ_EVENT command in 6.4 μs steps
OR_STRETCH	12–16	Defines layer-OR stretch in 50 ns steps
GTFE_CNT	7–11	Defines the number of GTFE chips to read
SIZE	0–6	Defines the maximum number of hits from GTFE

4 References

[1] LAT-TD-00156 LAT Tracker Preliminary Design Report
[2] LAT-SS-00017 LAT TKR Subsystem Specification — Level III Specification

[3] LAT-SS-00134 LAT TKR Subsystem Specification — Level IV Specification
[4] LAT-SS-00152 LAT TKR Subsystem Specification — Level IV Readout Electronics Requirements
[5] LAT-SS-00168 Conceptual Design of the LAT Tracker Electronics Readout System
[6] LAT-SS-00169 Tracker Front- End Readout ASIC Specification
[7] LAT-SS-00170 Conceptual Design of the GLAST Tracker Readout Controller Electronics ASIC (GTRC)
[8] LAT-SS-00171 Specification of the LAT Tracker front-end readout Multi-Chip Module (TMCM)
[11] LAT-TD-00153 Test Systems for the GLAST Tracker Front-End Electronics
[12] LAT-SS-00176 Tracker Electrical Interface Specification
[13] LAT-TD-00154 LAT Tracker Tray Test Plan
[14] LAT-TD-00155 LAT Tracker Tower Test Plan
[15] LAT-TD-00247 LAT Tracker Front-end Readout Chip Wafer Test Procedure
[16] LAT-TD-00249 GLAST LAT Tracker TMCM Test Procedures
[17] LAT-TD-00191 LAT Tracker Tower Electrical Test Plan

5 Tracker Tower Description

The conceptual design of the Tracker tower modules is described in the Preliminary Design Report[1]. The conceptual design of the read-out electronics is described in [5], and detailed specifications for the components of the design are found in [6], [7], [8], [9], and [10]. The electrical interface of the Tracker read-out to the TEM is described in [12].

The requirements for the Tracker electronics read-out are specified in [2], [3], and [4]. The tests described here refer to those documented requirements.

6 Test System

All of the tests described herein require the following ground support equipment: a probe card, an interface PWB with LVDS drivers/receivers, a VME I/O module, a VME-based ADC module, a VME Crate, a VME crate controller, a PC with a VEM interface card and a GPIB interface card, and power suppiles. The hardware configuration of the equipment is described in [11].

All the GTRC wafers are tested under a special condition/environment other than the normal operation condition/environment for GTRC chips in order to ensure effective screening of problematic chips with conservative safety margins. The test condition in the following table should be applied unless otherwise specified in the test procedures.

	Test condition	Normal operation
Clock frequency	25 MHz	20 MHz
Digital power supply voltage (DVDD)	2.2 V	2.5 V
Temperature	60 °C	—

7 Test Procedures

All the test procedures for GTRC chips in the GLAST LAT tracker construction is described below. A GTRC chip acts as a left-side controller or a right-side, depending on logic state of the LEFT pad (pin 9). Some of the tests should be performed only as a left-side controller, and the others should be repeated twice, once as a left-side controller and another time as a right-side controller. The former is designated by "LEFT only" in the test description, and the latter "LEFT and RIGHT".

7.1 Common Settings and Procedures

There are the settings and the procedures that should be applied to all the test procedures described in this section. Follow the instructions listed below in all the tests unless otherwise specified.

- Set 5 (0101 in binary) to a chip address (GTRC pins A0–A3) and to an address in a command, unless otherwise specified.
- Set 21 (10101 in binary) to a GTFE address in a command, unless otherwise specified.

- Use Event TAG 2 (two) for a trigger signal and for a simulated GTFE response, unless otherwise specified.
- Use buffer number 0 (zero) for a token, unless otherwise specified.
- Set 8 to the GTFE SYNC configuration register, unless otherwise specified.
- Attach correct parity bits to a GTRC command (a command parity and a data parity), a trigger signal, and a token.

7.2 Power Consumption Tests

7.2.1 Power Consumption

Test	TC101	**Direction**	LEFT only
Prerequisite	None		
Purpose	Measure the GTRC power consumption.		
Method	Measure the current draws into the power line (DVDD) and the current bias (DRV_BIAS).		
Specification	?? $< I_{\mathrm{DVDD}} <$??, and ?? $< I_{\mathrm{DRV\_IBIAS}} <$??. (The acceptance ranges are to be determined.)		

1. Supply 2.5 V on DVDD (digital power).
2. Supply a 20 MHz clock.
3. Measure the current draw into DVDD, and DRV_BIAS (current bias for LVDS drivers).
4. Record the current draws.
5. Confirm that the resulting current draws are within specifications.

7.2.2 LVDS quiescent output levels

Test	TC102	**Direction**	LEFT only
Prerequisite	Power test, TC101.		
Purpose	Measure the GTRC LVDS output levels.		
Method	Measure the voltages on the LVDS outputs of four types, both the P-sides and the M-sides, to obtain the mean voltages and the voltage differences between the pairs.		
Specification	Mean = 1.25±??, Diff. =??±?? for NTOKEN_OUTP/M, Diff. =??±?? for NSDATAP/M with address 0 (zero), Diff. =??±?? for NSDATAP/M with address 1-15, Diff. =??±?? for NTREQP/M, and Diff. =??±?? for CLKBP/M. (The acceptance ranges are to be determined.)		

1. Supply 2.5 V on DVDD (digital power).
2. Set a chip address to 0 (zero).
3. Measure the voltages of 8 selected pads: NTOKEN_OUTP, NTOKEN_OUTM, NSDATAP, NSDATAM, NTREQP, NTREQM, CLKBP, and CLKBM.
4. Confirm that the voltage differences between the LVDS pairs are appropriate levels for the driver types and modes: a programmable driver at its low-drive mode for NTOKEN_OUT, a programmable driver at its high-drive mode for NSDATA and NTREQ, a standard driver for CLKB.
5. Set a chip address to 1 (one).
6. Measure the voltages of 8 selected pads: NTOKEN_OUTP, NTOKEN_OUTM, NSDATAP, NSDATAM, NTREQP, NTREQM, CLKBP, and CLKBM.
7. Confirm that the voltage differences between the LVDS pairs are appropriate levels for the driver types and modes: a programmable driver at its low-drive mode for NTOKEN_OUT and NSDATA, a programmable driver at its high-drive mode for NTREQ, a standard driver for CLKB.
8. Repeat steps 5–7 for chip addresses of 2, 3, 4, ..., and 15.

7.3 Functionality Tests

7.3.1 SHIFT_MODE bit in the configuration register

Test	TC201	**Direction**	N/A
Prerequisite	Power test, TC101.		
Purpose	Test reading the SHIFT_MODE bit in the configuration register.		
Method	Hold the LEFT pad (pin 9) at a certain logic level and read out the configuration register.		
Specification	The SHIFT_MODE bit must store the logic level applied on the LEFT pad. The bit must be able to be set to 0 (zero) and to 1 (one). Read-back response must be in correct format with correct parities.		

1. Hold LEFT pad (pin 9) at logic high.
2. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
3. Check the bit stream to confirm that SHIFT_MODE bit is set to 1 (one).
4. Hold LEFT pad (pin 9) at logic low.
5. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
6. Check the bit stream to confirm that SHIFT_MODE bit is set to 0 (zero).

7.3.2 Configuration register load and read-back

Test	TC202	**Direction**	LEFT only
Prerequisite	Power test, TC101.		
Purpose	Test loading and reading back the configuration registers.		
Method	Load and read back the configuration registers.		
Specification	Register contents read back must be identical to those loaded. All the bits in the register must be able to be set to 0 (zero) and to 1 (one). Read-back response must be in correct format with correct parities.		

In this test, two sets of configuration register contents are applied: contents A & B in the table below. Both consist of ones and zeros alternating with each other in the configuration register. They are complement of each other to test all bits being set one and zero at least once each.

Name	Contents A	Contents B
TOT_EN	1	0
FORCE_NO_ERR	0	1
READ_DELAY	5 (101 in binary)	2 (010 in binary)
OR_STRETCH	10 (01010 in binary)	21 (10101 in binary)
GTFE_CNT	21 (10101 in binary)	10 (01010 in binary)
SIZE	42 (0101010 in binary)	85 (1010101 in binary)

1. Send a LD_GTRC_REG command with the following settings in its data bits.

Contents	LD_FT	LD_DELAY	LD_STRETCH	LD_CNT	LD_SIZE
A	1	1	1	1	1

2. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
3. Check the bit stream to confirm that contents A is set in the configuration register.
4. Repeat steps 1–2 with the following settings in its data bits.

Contents	LD_FT	LD_DELAY	LD_STRETCH	LD_CNT	LD_SIZE
B	1	0	0	0	0

5. Check the bit stream to confirm that only the part of contents B that is enabled loading is set in the configuration register, and that the other register contents remain unchanged since the previous loading.
6. Repeat steps 1–2 with the following settings in its data bits.

Contents	LD_FT	LD_DELAY	LD_STRETCH	LD_CNT	LD_SIZE
B	1	1	1	1	1

7. Check the bit stream to confirm that contents B is set in the configuration register.
8. Repeat steps 1–2 with the following settings in its data bits.

Contents	LD_FT	LD_DELAY	LD_STRETCH	LD_CNT	LD_SIZE
A	1	0	0	0	0

9. Check the bit stream to confirm that only the part of contents A that is enabled loading is set in the configuration register, and that the other register contents remain unchanged since the previous loading.
10. Repeat steps 1–2 with the following settings in its data bits.

Contents	LD_FT	LD_DELAY	LD_STRETCH	LD_CNT	LD_SIZE
A	1	1	1	1	1

11. Check the bit stream to confirm that contents A is set in the configuration register.
12. Repeat steps 1–11 with LD_FT and LD_DELAY swapped.
13. Repeat steps 1–11 with LD_FT and LD_STRETCH swapped.
14. Repeat steps 1–11 with LD_FT and LD_CNT swapped.
15. Repeat steps 1–11 with LD_FT and LD_SIZE swapped.

7.3.3 GTFE SYNC register load and read-back

Test	TC203	**Direction**	LEFT only
Prerequisite	Power test, TC101.		
Purpose	Test loading and reading back the GTFE SYNC registers.		
Method	Load and read back the configuration registers.		
Specification	Register contents read back must be identical to those loaded. All the bits in the register must be able to be set to 0 (zero) and to 1 (one). Read-back response must be in correct format with correct parities.		

1. Send a LD_GTFE_SYNC command to set 21 (10101 in binary) to the GTFE SYNC register.
2. Send a RD_GTFE_SYNC command and record a bit stream on NSDATA.
3. Confirm that the bit stream shows that the GTFE SYNC register stores 21.
4. Send a LD_GTFE_SYNC command to set 10 (01010 in binary) to the GTFE SYNC register.
5. Send a RD_GTFE_SYNC command and record a bit stream on NSDATA.
6. Confirm that the bit stream shows that the GTFE SYNC register stores 10.

7.3.4 Command forwarding

Test	TC204	**Direction**	LEFT only
Prerequisite	Power test, TC101.		
Purpose	Test sending GTFE commands through the GTRC chip.		
Method	Send a GTFE command and monitor the command output on the CMDB line.		
Specification	Commands on the output must be identical to the one on the input. All the possible function code (00000–11111 in binary) must be forwarded correctly. Command output must be in correct format with correct parities.		

1. Send a GTRC command of function code 00000 with GTFE_FUNC bit (the 5th bit of a command) set to 1 (one), and record a bit stream on SCMD_OUT.
2. Confirm that the bit stream includes only a GTFE command with the intended function code in a correct command format.
3. Repeat steps 1–2 for function codes 00001, 00010, 00011, 00100, 00101, 00110, 00111, 10000, 10001, 10010, 10011, 10100, 10101, 10110, 10111, 11000, 11001, 11010, 11011, 11100, 11101, 11110, and 11111.
4. Send a GTRC command of function code 01000 with GTFE_FUNC bit (the 5th bit of a command) set to 1 (one), including four sets of 10010010010010010 in series (68 bits in total) in its data field. Record a bit stream on SCMD_OUT.

5. Confirm that the bit stream includes only a GTFE command with the intended function code and the intended data field in a correct command format.
6. Repeat steps 4–5 for function codes 01001, 01010, 01011, 01100, 01101, 01110, and 01111.

7.3.5 CTRLREG echo

Test	TC205	**Direction**	LEFT only
Prerequisite	Command forwarding, TC204.		
Purpose	Test the CTRLREG input (pin 7).		
Method	Send a FE_RD_TRG_MSK command with a simulated GTFE response on the CTRLREG pad, and monitor the data output.		
Specification	Data output must be identical to the simulated GTFE response on CTRLREG. Data output must be in correct format with correct parities.		

1. Send a FE_RD_TRG_MSK command and record a bit stream on SCMD_OUT.
2. Confirm that a FE_RD_TRG_MSK command appears in the bit stream.
3. Place a simulated GTFE response on CTRLREG at the right time after the FE_RD_TRG_MSK command; the simulated response should be identical to mask register read-back from a GTFE in 68-bit data format showing channels 0, 3, 6, ..., 63 are unmasked. Record a bit stream on NSDATA.
4. Confirm that the bit stream contains the simulated GTFE response in a correct format.

7.3.6 Address decoding

Test	TC206	**Direction**	LEFT only
Prerequisite	Command forwarding, TC204.		
Purpose	Test the address decoding function.		
Method	Send a GTFE command with all the possible combinations of a hard-wired address and an address in the command, and monitor the command output.		
Specification	Command output must appear only in the cases in which the addresses given match or a read-out command is sent with a broadcast address. Command output must be in correct format with correct parities.		

1. Set 0 (zero) to a chip address (GTRC pins A0–A3).
2. Send 16 FE_RST_CHIP commands with GTRC addresses 0, 1, 2, ..., and 15, and record a bit stream on SCMD_OUT.
3. Confirm that a FE_RST_CHIP command appears in the bit stream only when the address in the command matches with the chip address set on pins A0–A3.
4. Repeat steps 1–3 for chip addresses 1, 2, 3, ..., and 15 set on pins A0–A3.

7.3.7 Read-out sequence

Test	TC207	**Direction**	LEFT & RIGHT
Prerequisite	SHIFT_MODE bit in the configuration register, TC201, Configuration register load and read-back, TC202, GTFE SYNC register load and read-back, TC203, and Address decoding, TC206.		
Purpose	Test the read-out function.		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, and monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence. The chip must take over the data output line while it is sending out the recorded event, and otherwise it must forward the data input to the data output. Data and command outputs must be in correct format with correct parities.		

1. Send a LD_GTRC_REG command to set the following contents.

TOT_EN	FORCE_NO_ERR	READ_DELAY	OR_STRETCH	GTFE_CNT	SIZE
1	0	0	10	12	64

2. Send a LD_GTFE_SYNC command to set 8 to the GTFE SYNC register.
3. Place a 7 μs-wide pulse of on TREQ_IN and a trigger signal on NTACK; the trigger signal should be placed 1 μs after the leading edge of the pulse on TREQ_IN. Record a logic state of NTREQ and a bit stream on TACKB.
4. Confirm that NTREQ outputs a 7.5 μs-wide pulse in response to the pulse on TREQ_IN. Note that the pulse on NTREQ should be 10 clock cycles longer than that on TREQ_IN due to OR_STRETCH.
5. Confirm that the bit stream on TACKB includes a trigger signal, that is identical to the one on NTACK, appearing with no delay.
6. Place a simulated data packet, which is a bit stream of ones and zeros alternating each other, on NSDATA_IN; it should be kept on NSDATA_IN until the end of this test. Start recording bit streams on NSDATA and NTOKEN_OUT.
7. Send a READ_EVENT command and record a bit stream on SCMD_OUT.
8. Confirm that a READ_EVENT command appears in the bit stream.
9. Place a simulated response of 12 GTFE chips on RD_IN at the right time after the READ_EVENT command. The simulated response should include the 64 hits as in the following table.

GTFE chip	Hits on
1st chip	channels 0, 12, 24, 36, 48, and 60
2nd chip	channels 1, 13, 25, 37, 49, and 61
3rd chip	channels 2, 14, 26, 38, 50, and 62
4th chip	channels 3, 15, 27, 39, 51, and 63
5th chip	channels 4, 16, 28, 40, and 52
6th chip	channels 5, 17, 29, 41, and 53
7th chip	channels 6, 18, 30, 42, and 54
8th chip	channels 7, 19, 31, 43, and 55
9th chip	channels 8, 20, 32, 44, and 56
10th chip	channels 9, 21, 33, 45, and 57
11th chip	channels 10, 22, 34, 46, and 58
12th chip	channels 11, 23, 35, 47, and 59

10. Place a token on NTOKEN after the end of the READ_EVENT command.
11. Terminate recording bit streams on NSDATA and NTOKEN_OUT 20 clock cycles after the end of the data packet of the event stored in the tested GTRC chip.
12. Confirm that the bit stream on NSDATA starts with the alternating pattern, followed by the data packet containing the simulated hits in a correct format for normal operation mode with data, and ends with the alternating pattern.
13. Confirm that a token appears in the bit stream on NTOKEN_OUT at the right time.
14. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
15. Confirm that the bit stream shows that no error bit is set in the configuration register.

7.3.8 TOT-delay setting

Test	TC208	**Direction**	LEFT only
Prerequisite	Read-out sequence, TC207.		
Purpose	Test the TOT delay function (TOT_EN bit in the configuration register).		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with the trigger request kept high until a hundred clock-cycles after the READ_EVENT command completes. Monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence; with TOT_EN bit set to 1 (one), the chip must send out a data packet after the trigger request goes down; with TOT_EN bit set to 0 (zero), it must send out a data packet immediately after the READ_EVENT command without waiting for the trigger request to go down. Data and command outputs must be in correct format with correct parities.		

1. Repeat read-out test TC207 with the following settings:
   - TOT_EN in the configuration register is set to 0.
   - The TREQ_IN pulse is longer than the simulated GTFE response, e.g., of 50 μs long.
   - The token is passed before the end of the simulated GTFE response.
2. Confirm that the data packet comes out on NSDATA immediately after a token is passed.
3. Repeat read-out test TC207 with the following settings:
   - TOT_EN in the configuration register is set to 1.
   - The TREQ_IN pulse is longer than the simulated GTFE response, e.g., 50 μs long.
   - The token is passed before the end of the simulated GTFE response.
4. Confirm that the data packet comes out on NSDATA after the end of the TREQ_IN pulse.

7.3.9 Read-delay setting

Test	TC209	**Direction**	LEFT only
Prerequisite	Read-out sequence, TC207.		
Purpose	Test the read-delay function (READ_DELAY bits in the configuration register).		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with various numbers set to READ_DELAY, and monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence, with the intended delay between the READ_EVENT command and the FE_READ_EVENT command. Data and command outputs must be in correct format with correct parities.		

1. Repeat read-out test TC207 for read-delays of 0, 1, 2, ..., and 7 to be set to READ_DELAY bits in the configuration register.
2. Confirm that a FE_READ_EVENT comes out on SCMD_OUT $128nT$ μs after the end of READ_EVENT command, where where T is the clock period in μs and n is the number set to READ_DELAY.

7.3.10 OR-stretch setting

Test	TC210	**Direction**	LEFT only
Prerequisite	Read-out sequence, TC207.		
Purpose	Test the layer-OR stretch function (OR_STRETCH bits in the configuration register).		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with various settings for OR_STRETCH, and measure the length of a pulse on the layer-OR output.		
Specification	The layer-OR signal on the output must be stretched by the intended amount. Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence. Data and command outputs must be in correct format with correct parities.		

1. Repeat read-out test TC207 for OR-stretches of 0, 1, 2, ..., and 31 to be set to OR_STRETCH bits in the configuration register.
2. Confirm that the length of a pulse on NTREQ is $(7 + nT)$ μs long, where T is the clock period in μs and n is the number set to OR_STRETCH.

7.3.11 Number-of-chips-to-read setting

Test	TC211	**Direction**	LEFT & RIGHT
Prerequisite	Read-out sequence, TC207.		
Purpose	Test limiting the number of chips to read-out (GTFE_CNT bits in the configuration register).		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with various numbers set to GTFE_CNT, and monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Only the intended number of the simulated GTFE chips must be read out. Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence. Data and command outputs must be in correct format with correct parities.		

1. Repeat read-out test TC207 with the following settings:
   - GTFE_CNT in the configuration register is set to 0, 1, 2, ..., and 24.
   - The simulated GTFE response should include the 64 hits as in the following table.

GTFE chip	Hits on
1st chip	channels 0, 24, and 48
2nd chip	channels 1, 25, and 49
3rd chip	channels 2, 26, and 50
4th chip	channels 3, 27, and 51
5th chip	channels 4, 28, and 52
6th chip	channels 5, 29, and 53
7th chip	channels 6, 30, and 54
8th chip	channels 7, 31, and 55
9th chip	channels 8, 32, and 56
10th chip	channels 9, 33, and 57
11th chip	channels 10, 34, and 58
12th chip	channels 11, 35, and 59
13th chip	channels 12, 36, and 60
14nd chip	channels 13, 37, and 61
15rd chip	channels 14, 38, and 62
16th chip	channels 15, 39, and 63
17th chip	channels 16, and 40
18th chip	channels 17, and 41
19th chip	channels 18, and 42
20th chip	channels 19, and 43
21th chip	channels 20, and 44
22th chip	channels 21, and 45
23th chip	channels 22, and 46
24th chip	channels 23, and 47

2. Confirm that only the intended number of GTFE chips are read out, i.e., only the hits on these GTFE's appear in a data packet on NSDATA.
3. Repeat steps 1–2 with LEFT (GTRC pin 9) held at logic low throughout the steps.

7.3.12 Maximum-number-of-hits setting

Test	TC212	**Direction**	LEFT & RIGHT
Prerequisite	Read-out sequence, TC207.		
Purpose	Test limiting the number of hits to read-out (SIZE bits in the configuration register).		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with various numbers set to SIZE, and monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Only the intended number of the simulated hits must be read out. Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence. Data and command outputs must be in correct format with correct parities.		

1. Repeat read-out test TC207 for the maximum numbers of hits of 0, 1, 2, ..., and 64 to be set to SIZE bits in the configuration register.
2. Confirm that only the intended number of hits appear in a data packet on NSDATA.
3. Repeat steps 1–2 with LEFT (GTRC pin 9) held at logic low throughout the steps.

7.3.13 GTFE SYNC register setting

Test	TC213	**Direction**	LEFT Only
Prerequisite	Read-out sequence, TC207.		
Purpose	Test changing GTFE SYNC setting (GTFE SYNC register).		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with various numbers set to GTFE SYNC, and monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence for all GTFE SYNC values. Data and command outputs must be in correct format with correct parities.		

1. Repeat read-out test TC207 for GTFE SYNC of 0, 1, 2, ..., and 31 to be set to the GTFE SYNC register, with an appropriate delay of simulated response of GTFE chips.
2. Confirm that the tested GTRC chip responds as in TC207.

7.3.14 Hard and soft reset

Test	TC214	**Direction**	LEFT & RIGHT
Prerequisite	Read-out sequence, TC207.		
Purpose	Test the hard and soft reset functions.		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, with various numbers set to SIZE, and monitor the command, data, token, trigger-request, and trigger-acknowledge outputs. The reset is initiated by a reset command and a reset pulse.		
Specification	The chip must stop sending out the data immediately when the reset becomes in effect. No hit must be reported in case that the reset is issued during data transfer between GTFE and GTRC. Register contents must be set to the power-on default. Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence until the reset becomes in effect.		

1. Repeat read-out test TC207 with a reset pulse placed on NRESET while the tested chip is sending out a data packet. Record a bit stream on RESETB.
2. Confirm that a reset pulse appears on RESETB in response to the reset pulse on NRESET.
3. Confirm that the tested chip stops sending out the data packet in response to the reset pulse on NRESET.
4. Send a RD_GTRC_REG command and a RD_GTFE_SYNC command, and record a bit stream on NSDATA.
5. Confirm that contents of the configuration register and the GTFE SYNC register are reset to the power-on default.
6. Repeat read-out test TC207 with a reset pulse placed on NRESET while the simulated GTFE response is being sent to the tested chip and before the tested chip sends out a data packet. Record a bit stream on RESETB.
7. Confirm that a reset pulse appears on RESETB in response to the reset pulse on NRESET.
8. Repeat steps 4–5.
9. Confirm that the tested chip does not send out the data packet in response to the reset pulse on NRESET.
10. Repeat steps 1–9 by sending a RST_GTRC command instead of a reset pulse. Note that a pulse on RESETB will not appear.

7.3.15 Error detection

Test	TC215	**Direction**	LEFT only
Prerequisite	CTRLREG echo, TC205, and Read-out sequence, TC207.		
Purpose	Test the error detection function.		
Method	Simulate a set of error-causing inputs and read out the configuration register to check the errors.		
Specification	Corresponding error-bit(s) must be set. Error bits must be clear by a RD_GTRC_REG command. Data and command outputs must be in correct format with correct parities.		

1. Send a RD_GTRC_REG command to clear the error(s).
2. Send a RST_GTRC command with the wrong command parity.
3. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
4. Confirm that the bit stream shows that SUM_ERR and CMD_ERR are set to 1; note that there are two bits reporting SUM_ERR in the response and both must be set to 1 (one).
5. Send a LD_GTFE_SYNC command to set 21 (10101 in binary) to the GTFE SYNC register.
6. Send a RD_GTFE_SYNC command and record a bit stream on NSDATA.
7. Confirm that the bit stream shows that the GTFE SYNC register stores 21 and that SUM_ERR is set to 0 (zero).
8. Send a LD_GTFE_SYNC command to set 10 (01010 in binary) to the GTFE SYNC register with the wrong data parity.
9. Send a RD_GTFE_SYNC command and record a bit stream on NSDATA.
10. Confirm that the bit stream shows that the GTFE SYNC register still stores 21 and that SUM_ERR is set to 1 (one).
11. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
12. Confirm that the bit stream shows that SUM_ERR and DAT_ERR are set to 1; note that there are two bits reporting SUM_ERR in the response and both must be set to 1 (one).
13. Send a FE_RD_TRG_MSK command with the wrong command parity. Place a simulated GTFE response on CTRLREG at the right time after the FE_RD_TRG_MSK command; the simulated response should be a bit stream of four sets of 10010010010010010 in series (68 bits in total). Record a bit stream on NSDATA.
14. Confirm that the bit stream contains the simulated GTFE response in a correct format and the SUM_ERR set to 1.
15. Send a RD_GTRC_REG command to clear the error(s) and record a bit stream on NSDATA.
16. Confirm that the bit stream shows that SUM_ERR and DAT_ERR are set to 1; note that there are two bits reporting SUM_ERR in the response and both must be set to 1 (one).
17. Send a FE_LD_TRG_MSK command with the wrong data parity. Use four sets of 10010010010010010 in series (68 bits in total) for data to load. Record a bit stream on NSDATA.
18. Confirm that the bit stream contains the simulated GTFE response in a correct format and the SUM_ERR set to 1.
19. Send a RD_GTRC_REG command to clear the error(s) and record a bit stream on NSDATA.
20. Confirm that the bit stream shows that SUM_ERR and DAT_ERR are set to 1; note that there are two bits reporting SUM_ERR in the response and both must be set to 1 (one).
21. Place a trigger signal on NTACK with the wrong trigger parity.
22. Send a RD_GTRC_REG command and record a bit stream on NSDATA.
23. Confirm that the bit stream shows that SUM_ERR and TRIG_ERR are set to 1.
24. Place a token on NTOKEN with the wrong token parity.
25. Send a RD_GTRC_REG command and record a bit stream on NSDATA.

26. Confirm that the bit stream shows that SUM_ERR and TOK_ERR are set to 1.
27. Repeat read-out test TC207 with the wrong TAG's in the simulated GTFE response.
28. Confirm that the bit stream shows that SUM_ERR and TAG_ERR are set to 1.

7.3.16 Error handling

Test	TC216	**Direction**	LEFT only
Prerequisite	Read-out sequence, TC207.		
Purpose	Test data read-out behavior in case of errors, with FORCE_NO_ERR bit in the configuration register set and with the bit unset.		
Method	Initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, which includes error-causing contents. Monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence. Data and command outputs must be in correct format for a combination of error status and FORCE_NO_ERR bit setting with correct parities.		

1. Repeat read-out test TC207 with the wrong TAG's in the simulated GTFE response.
2. Confirm that the data packet coming out of the tested chip (the bit stream on NSDATA) is in a correct format for error mode with data.
3. Repeat read-out test TC207 with the wrong TAG's in the simulated GTFE response and with the FORCE_NO_ERR bit in the configuration register set to 1 (one).
4. Confirm that the data packet coming out of the tested chip (the bit stream on NSDATA) is in a correct format for normal operation mode with data.
5. Repeat read-out test TC207 with the a simulated GTFE response containing no hits.
6. Confirm that the data packet coming out of the tested chip (the bit stream on NSDATA) is in a correct format for normal operation mode without data.
7. Repeat read-out test TC207 with the wrong TAG's in the simulated GTFE response containing no hits.
8. Confirm that the data packet coming out of the tested chip (the bit stream on NSDATA) is in a correct format for error mode without data.
9. Repeat read-out test TC207 with the wrong TAG's in the simulated GTFE response containing no hits and with the FORCE_NO_ERR bit in the configuration register set to 1 (one).
10. Confirm that the data packet coming out of the tested chip (the bit stream on NSDATA) is in a correct format for normal operation mode without data.

7.3.17 Response to undefined commands

Test	TC217	**Direction**	LEFT only
Prerequisite	Read-out sequence, TC207.		
Purpose	Test chip response to undefined commands.		
Method	After sending an undefined command, initiate a read-out sequence with simulated response of GTFE's, GTRC's, and a TEM, which includes error-causing contents. Monitor the command, data, token, trigger-request, and trigger-acknowledge outputs.		
Specification	Commands, data, tokens, trigger requests, and trigger acknowledges must appear at the right time during a read-out sequence. Data and command outputs must be in correct format with correct parities.		

1. Send a command with function code 00000 with GTFE_FUNC bit (the 5th bit of a command) set to 0 (zero) and with a dummy 68-bit data.
2. Repeat read-out test TC207.
3. Confirm the correct data read-out sequence.

4. Repeat steps 1–3 for function codes 00010, 00011, 00101, 00110, 00111, 01010, 01011, 01100, 01101, 01110, 01111, 10010, 10011, 10100, 10101, 10110, 10111, 11000, 11001, 11010, 11011, 11100, 11101, 11110, and 11111. Note that no dummy data should be attached for function codes 01xxx.

8 Chip Rating and Acceptance Criteria

All tested GTRC chips are rated in three ranks based on the test results. Depending on its chip rating, a tested chip is to be assembled onto a TMCM, rejected from the assembly (unused at all), or stored as spares for future use. The three ranks are described below.

"Good" Chips that pass all the test described in this document are rated "good". Chips rated "good" are to primarily be assembled onto TMCM's.

"Spare" Chips that pass all the test described in this document except for one of the following cases:

- CMD_ERR bit in the configuration register stays high and FORCE_NO_ERR bit in the configuration register functions.
- DAT_ERR bit in the configuration register stays high and FORCE_NO_ERR bit in the configuration register functions.
- TRIG_ERR bit in the configuration register stays high and FORCE_NO_ERR bit in the configuration register functions.
- TOK_ERR bit in the configuration register stays high and FORCE_NO_ERR bit in the configuration register functions.
- TAG_ERR bit in the configuration register stays high and FORCE_NO_ERR bit in the configuration register functions.

Chips rated "spare" are to be assembled onto TMCM's if and only if the number of good chips is not sufficient to produce sufficient number of TMCM's.

"Reject" Chips that are not rated either "good" or "spare" are rated "reject". Chips rated "reject" are not to be assembled onto TMCM's.